

OUTLINE

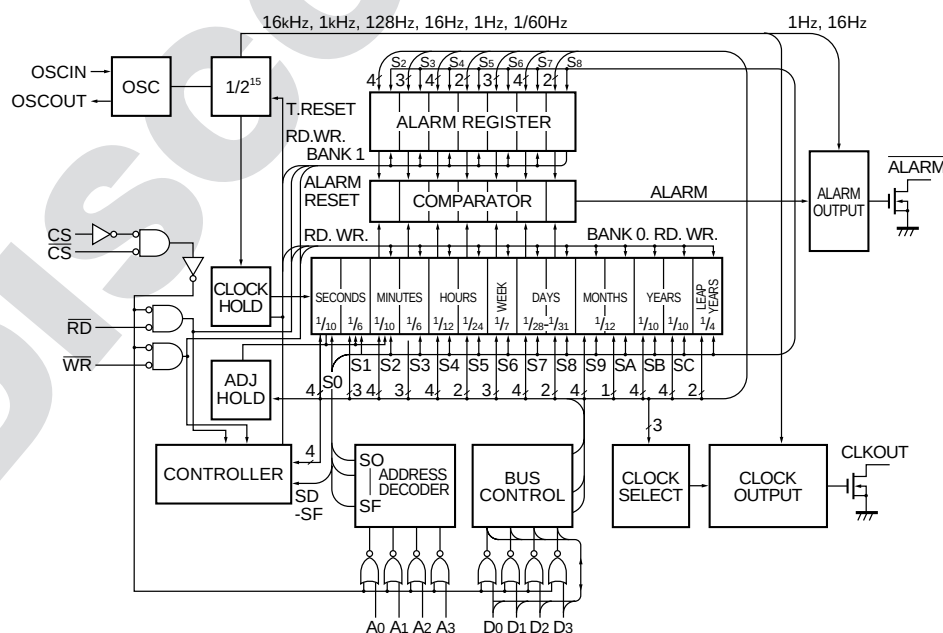
The RP/RF/RJ5C15 are real-time clocks for microcomputers that can be connected directly to data buses of 16bit CPUs, such as the 8086, Z8000, and 68000, and of 8bit CPUs, such as the 8085A, Z80, 6809, and 6502. They allow setting or reading of the clock with the same procedures as for the Read/Write operation for memory.

These products have various features including clock, calendar and alarm functions and can be backed up by batteries.

FEATURES

- Connected directly to CPU enabling fast access.
- 4bit bidirectional data bus : D0 - D3
- 4bit address input : A0 - A3
- Built-in clock counter (hour, minute, second) and calendar counter (leap year, year, month, day, day-of-the-week)
- All clock data expressed in BCD codes
- Backed up by batteries (minimum : 2.0V)
- Selectable basic clock frequency : 16kHz, 1kHz, 128Hz, 16Hz, 1Hz, 1/60Hz.
- Outputs alarm signals or timing pulse of 16Hz or 1Hz.
- CMOS technology
- Supply voltage : Single power supply of +5V
- Packages RP5C15.....18pin DIP
RF5C15.....18pin SOP
RJ5C15.....28pin PLCC

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Item	Conditions	Ratings	Unit
V _{CC}	Supply Voltage		−0.3 to 7.0	V
V _I	Input Voltage	Referenced at GND pin	−0.3 to V _{CC} +0.3	V
V _O	Output Voltage		−0.3 to V _{CC} +0.3	V
P _d	Maximum Power Dissipation	T _a =25°C	400	mW
T _{opr}	Operating Temperature		−20 to 70	°C
T _{stg}	Storage Temperature		−40 to 125	°C

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum ratings are threshold limit values that must not be exceeded even for an instant under any conditions. Moreover, such values for any two items must not be reached simultaneously. Operation above these absolute maximum ratings may cause degradation or permanent damage to the device. These are stress ratings only and do not necessarily imply functional operation below these limits.

RECOMMENDED OPERATING CONDITIONS

(Unless otherwise specified, T_a=−20 to 70°C)

Symbol	Item	Conditions	MIN.	TYP.	MAX.	Unit
V _{CC}	Supply Voltage		4.5	5	5.5	V
V _{DH}	Data Preservation Voltage		2.0		5.5	V
f _{XT}	Crystal Oscillation Frequency			32.768		kHz

DC ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, Ta=−20 to 70°C, Vcc=5V±10%)

Symbol	Item	Conditions	MIN.	TYP.	MAX.	Unit
VIH	“H” Input Voltage (excluding OSCIN)		2.0		Vcc+0.3	V
	“H” Input Voltage (OSCIN)		2.4		Vcc+0.3	V
VIL	“L” Input Voltage (excluding OSCIN)		−0.3		0.8	V
	“L” Input Voltage (OSCIN)		−0.3		0.5	V
VOH	“H” Output Voltage	IOH=−400μA	2.4			V
VOL	“L” Output Voltage	IOL=2mA			0.4	V
ILI	Input Leakage Current	VIN=0 to Vcc	−10		10	μA
IOZ	Output Off-state Leakage Current	Voz=0 to 5.5V			±10	μA
ICC1	Supply Current for Backup	fXT=32.768kHz, Vcc=2.0V			15	μA
ICC2	Operating Supply Current	fXT=32.768kHz, Vcc=5.5V*			250	μA
VILCS	CS pin “L” Input Voltage for Backup	Vcc=2.0V	−0.2		0.2	V
VIHCS	CS pin “H” Input Voltage for Backup	Vcc=2.0V	1.8		2.0	V

★) RD, WR signal frequency : 100kHz ; Input pin is fixed at Vcc or GND level ; output pin open.

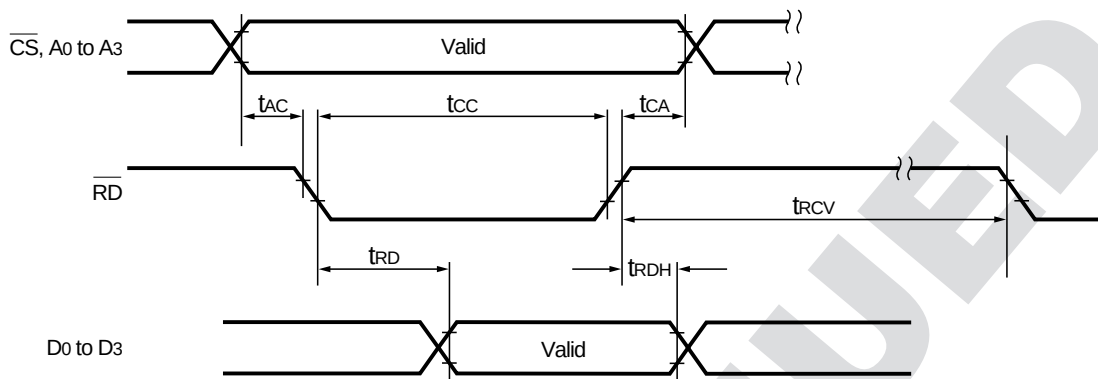
AC ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, Ta=−20 to 70°C, Vcc=5V±10%)

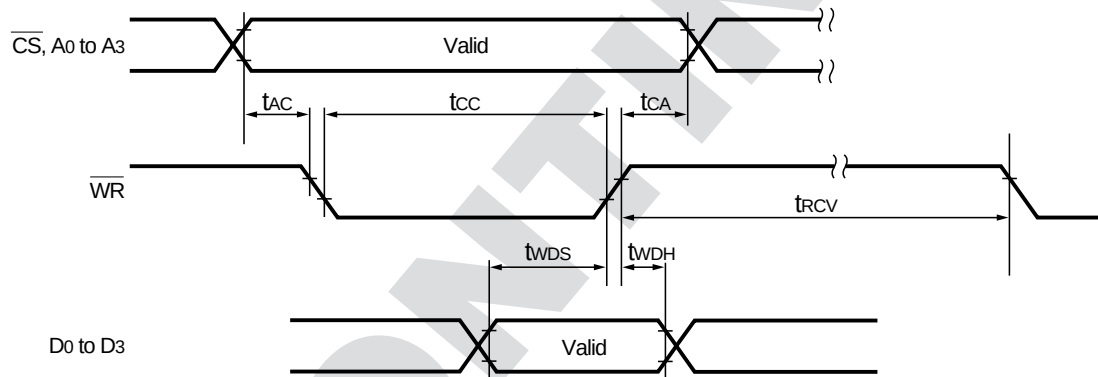
Symbol	Item	Conditions	MIN.	TYP.	MAX.	Unit
tAC	Address $\overline{\text{RD}}$ / $\overline{\text{WR}}$ Delay Time		50			ns
tCC	$\overline{\text{RD}}$ / $\overline{\text{WR}}$ Pulse Width		120		13000	ns
tCA	Address Effective Time after rising of $\overline{\text{RD}}$ / $\overline{\text{WR}}$		10			ns
tRD	Data Delay Time after falling of $\overline{\text{RD}}$	1TTL+100pF			120	ns
tRDH	Data Hold Time after rising of $\overline{\text{RD}}$		10			ns
tWDS	Data Setup Time in Write operation		100			ns
tWDH	Data Hold Time in Write operation		20			ns
tTED	Timer Enable to Timer Disable		100			μs
tADJ	Adjust Completion Time				100	μs
tAINH	Alarm Write Inhibit Time after Resetting		100			μs
tRCV	$\overline{\text{RD}}$ / $\overline{\text{WR}}$ Recovery Time		1			μs

TIMING CHART

• Read Cycle



• Write Cycle



ADDRESS MAPPING

MODE	BANK 0					BANK 1				
A3 to A0	Description	D3	D2	D1	D0	Description	D3	D2	D1	D0
0	1-second counter					Clock output select register	×			
1	10-second counter	×				Adjust	×	×	×	ADJ
2	1-minute counter					1-minute alarm register				
3	10-minute counter	×				10-minute alarm register	×			
4	1-hour counter					1-hour alarm register				
5	10-hour counter	×	×			10-hour alarm register	×	×		
6	Day-of-the-week counter	×				Day-of-the-week alarm register	×			
7	1-day counter					1-day alarm register				
8	10-day counter	×	×			10-day alarm register	×	×		
9	1-month counter						×	×	×	×
A	10-month counter	×	×	×		12/24 select register	×	×	×	
B	1-year counter					Leap year counter	×	×		
C	10-year counter						×	×	×	×
D	MODE register	Timer EN	Alarm EN	×	BANK1/0		Timer EN	Alarm EN	×	BANK1/0
E	TEST register	Test 3	Test 2	Test 1	Test 0		Test 3	Test 2	Test 1	Test 0
F	RESET controller, etc.	1Hz ON	16Hz ON	Timer RESET	Alarm RESET		1Hz ON	16Hz ON	Timer RESET	Alarm RESET

★) "x" means "Don't care" for Write ; always "0" for Read.

• Clock Output Select Register (BANK 1, Address 0h)

D3	D2	D1	D0	Clock Output	Remarks
×	0	0	0	"Z"	High impedance
×	0	0	1	16.384kHz	duty 50%
×	0	1	0	1.024kHz	duty 50%
×	0	1	1	128Hz	duty 50%
×	1	0	0	16Hz	duty 50%
×	1	0	1	1Hz	duty 50% ⌋ When the second counter counts up.
×	1	1	0	1/60Hz	duty 50% ⌋ When the second counter counts up.
×	1	1	1	"L"	

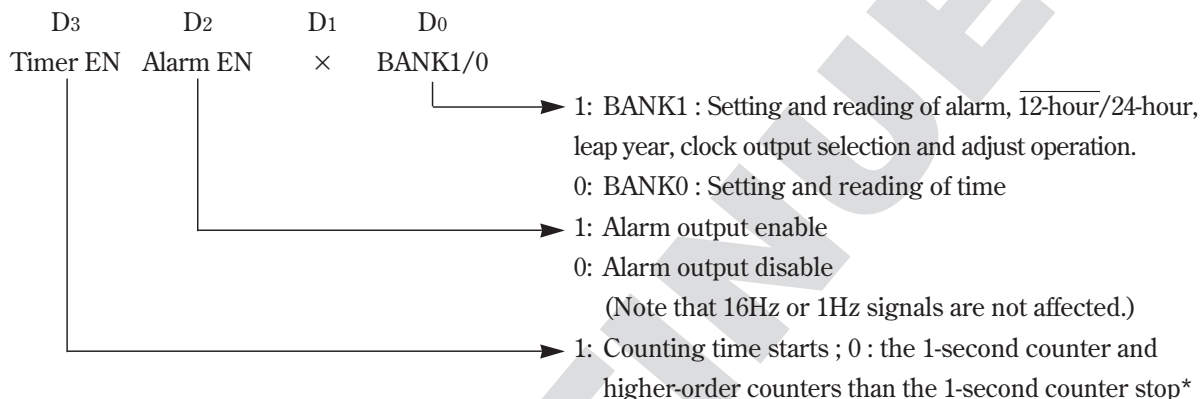
★) "x" means "Don't care" for Write ; always "0" for Read.

- **ADJ (BANK1, Address 1h, D0)**

Bit for correcting the second digit. When set to 1,

- 1) For digits ranging from 00 to 29 : Resets the lower-order counter than the 1-second counter and sets the second digit to 00.
- 2) For digits ranging from 30 to 59 : Resets the lower-order counter than the 1-second counter, sets the second digit to 00 and increments the minute digit by 1.

- **MODE register (BANK1/0, Address Dh)**



*) When the Timer EN is set to 0, the 1-second counter and higher-order counters than the 1-second counter stop. If any carrying occurs in the lower-order counters than the 1-second counter while the Timer EN is 0, carrying will be held and avoided until the Timer EN changes from 0 to 1. Thus, no apparent delay is produced when the duration of the Timer EN = 0 is less than one second.

- **12/24 select register (BANK1, Address Ah)**

D0=1 sets to 24-hour system ; D0=0 sets to 12-hour system.

Set the 10-hour counter as D1=1 for p.m., D1=0 for a.m.

- **Leap year counter (BANK1, Address Bh)**

(D1, D0)=(0, 0) sets the counter for leap years. The counter value changes in the order of (0, 0) (0, 1) (1, 0) (1, 1) (0, 0) repeatedly in the same timing as the year counter.

- **RESET controller/16Hz · 1Hz clock register. (BANK1/0, Address Fh)**

D0=1 : Resets all alarm registers.

D1=1 : Resets divider stages for seconds or smaller units.

D2=0 : 16Hz clock pulse ON.

D3=0 : 1Hz clock pulse ON.

- **Test register (BANK1/0, Address Eh)**

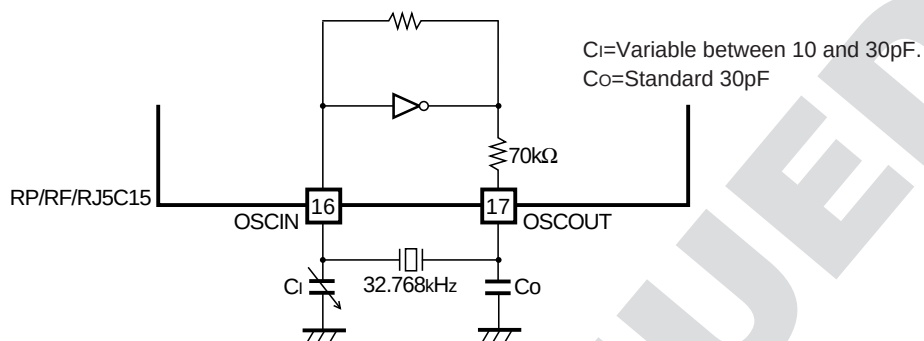
Register used for LSI inspection. Recommended setting is (D3, D2, D1, D0)=(0, 0, 0, 0)

*) Addresses 0h to Dh are applicable both for Read and Write.

*) Addresses Eh to Fh are applicable only for Write.

OSCILLATOR CIRCUIT

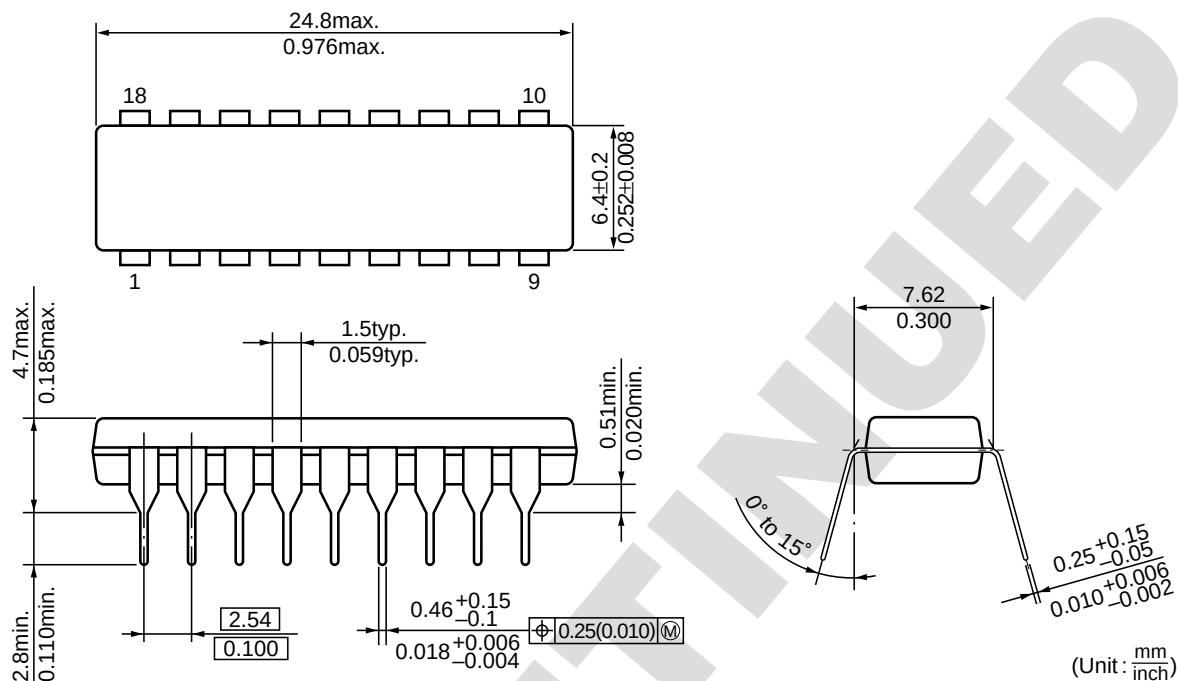
Since this circuit includes an output ballast resistor ($\approx 70k$), no external device is necessary.



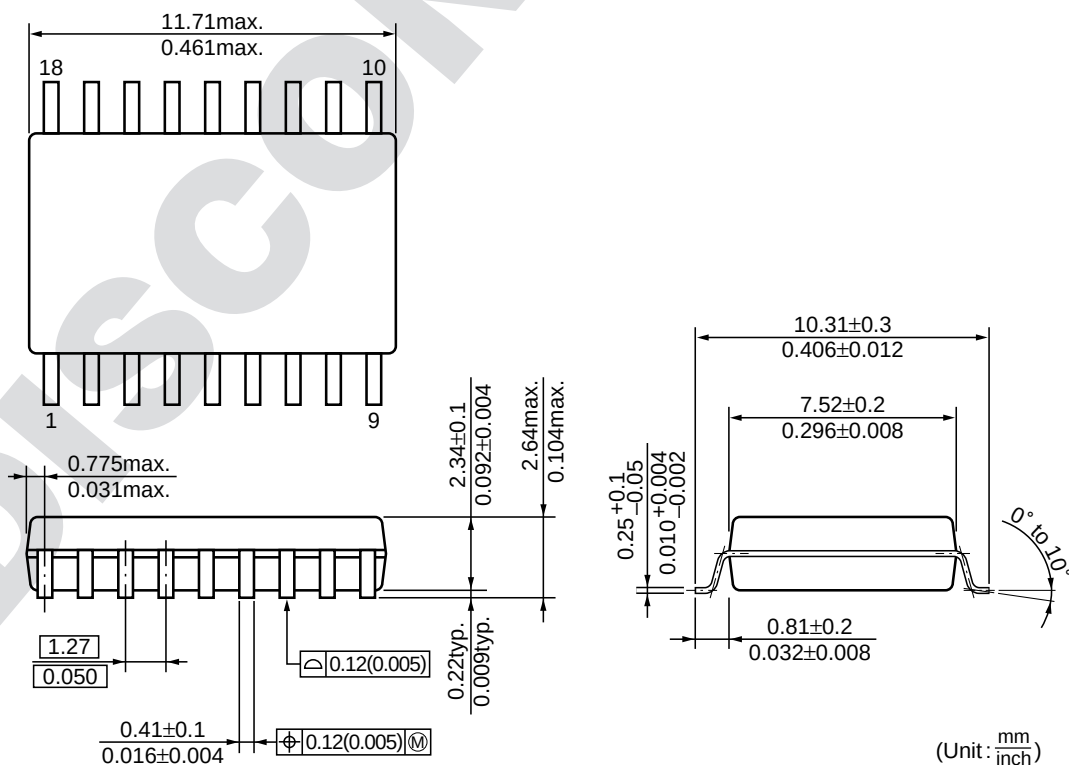
- ★) Values of C_1 and C_o are for reference only.
- ★) In the RJ5C15, the OSCIN is 26pin and the OSCOUT is 27pin.

PACKAGE DIMENSIONS

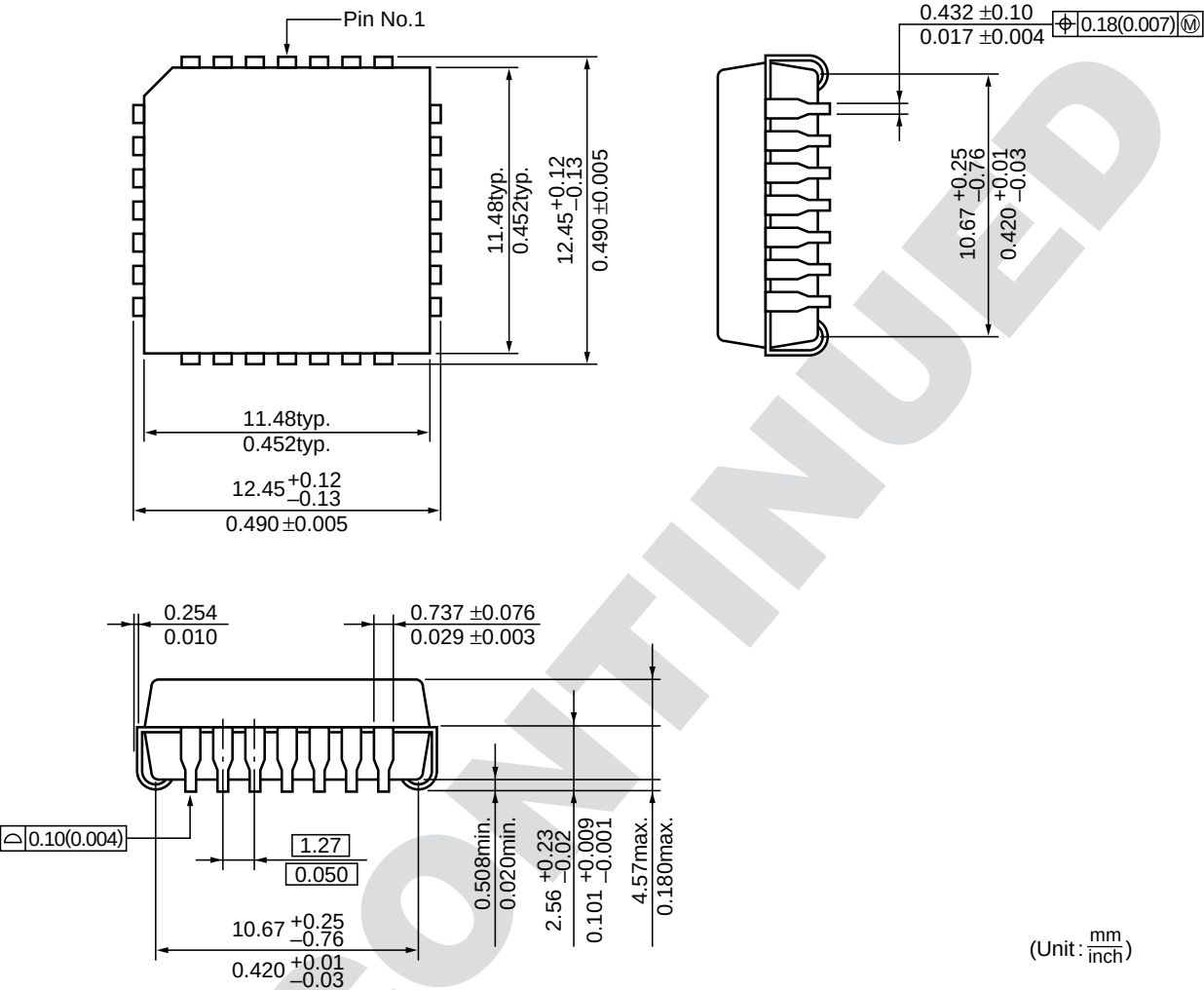
• RP5C15 (18pin DIP)



• RF5C15 (18pin SOP)



• RJ5C15 (24pin PLCC)



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